

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 7,224,029 B2  
APPLICATION NO. : 10/707964  
DATED : May 29, 2007  
INVENTOR(S) : Anderson et al.

Page 1 of 17

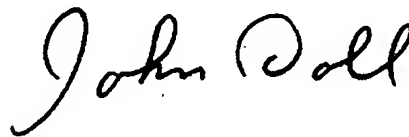
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

The title page showing the illustrative figure should be deleted to be replaced with the attached title page.

The drawing sheets, consisting of Figs. 1A-15, should be deleted to be replaced with the drawing sheets, consisting of Figs. 1A-15, as shown on the attached page.

Signed and Sealed this

Seventeenth Day of February, 2009



JOHN DOLL  
*Acting Director of the United States Patent and Trademark Office*

(12) **United States Patent**  
Anderson et al.

(10) Patent No.: **US 7,224,029 B2**  
(45) Date of Patent: **May 29, 2007**

(54) **METHOD AND STRUCTURE TO CREATE  
MULTIPLE DEVICE WIDTHS IN FINFET  
TECHNOLOGY IN BOTH BULK AND SOI**

(75) Inventors: **Brent A. Anderson, Jericho, VT (US);  
Edward J. Nowak, Essex Junction, VT  
(US); Jed H. Rankin, Essex Junction,  
VT (US)**

(73) Assignee: **International Business Machines  
Corporation, Armonk, NY (US)**

(\*) Notice: Subject to any disclaimer, the term of this  
patent is extended or adjusted under 35  
U.S.C. 154(b) by 66 days.

(21) Appl. No.: **10/707,964**

(22) Filed: **Jan. 28, 2004**

(65) **Prior Publication Data**  
**US 2005/0161739 A1 Jul. 28, 2005**

(51) Int. Cl.  
**H01L 21/36 (2006.01)**  
**H01L 27/01 (2006.01)**

(52) U.S. Cl. .... **257/347; 257/350; 257/351;  
257/369; 257/344; 257/296**

(58) Field of Classification Search ..... **257/200,  
257/201, 202, 207, 205, 349, 350, 351, 374,  
257/208, 369, 370, 371, 376**  
See application file for complete search history.

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

**5,739,057 A 4/1998 Tiwari et al.**  
**6,342,410 B1 1/2002 Yu**

**6,432,829 B2 8/2002 Muller**  
**6,475,890 B1 11/2002 Yu**  
**6,492,212 B1 12/2002 Jeong et al.**  
**6,525,403 B2 2/2003 Inaba et al.**  
**6,562,665 B1 5/2003 Yu**  
**6,756,643 B1\* 6/2004 Achuthan et al. .... 257/365**  
**6,787,406 B1\* 9/2004 Hill et al. .... 438/164**  
**2003/0042531 A1 3/2003 Lee et al.**  
**2003/0102518 A1 6/2003 Fried et al.**  
**2003/0113970 A1 6/2003 Fried et al.**  
**2003/0193058 A1\* 10/2003 Fried et al. .... 257/200**

\* cited by examiner

*Primary Examiner—Evan Pert*

*Assistant Examiner—Fazli Erdem*

*(74) Attorney, Agent, or Firm—Gibb I.P. Law Firm, LLC;  
William D. Sabo, Esq.*

(57) **ABSTRACT**

Disclosed is a structure and method for producing a fin-type field effect transistor (FinFET) that has a buried oxide layer over a substrate, at least one first fin structure and at least one second fin structure positioned on the buried oxide layer. First spacers are adjacent the first fin structure and second spacers are adjacent the second fin structure. The first spacers cover a larger portion of the first fin structure when compared to the portion of the second fin structure covered by the second spacers. Those fins that have larger spacers will receive a smaller area of semiconductor doping and those fins that have smaller spacers will receive a larger area of semiconductor doping. Therefore, there is a difference in doping between the first fins and the second fins that is caused by the differently sized spacers. The difference in doping between the first fins and the second fins changes an effective width of the second fins when compared to the first fins.

**11 Claims, 15 Drawing Sheets**

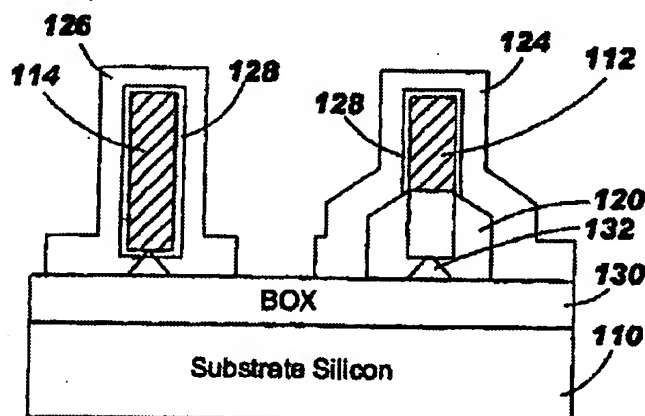


FIG. 1A

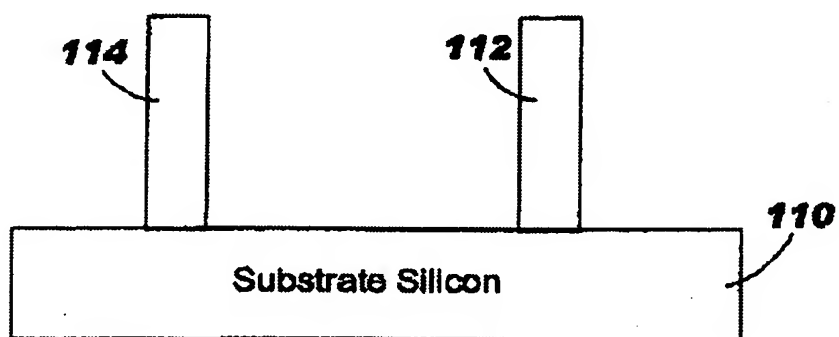


FIG. 1B

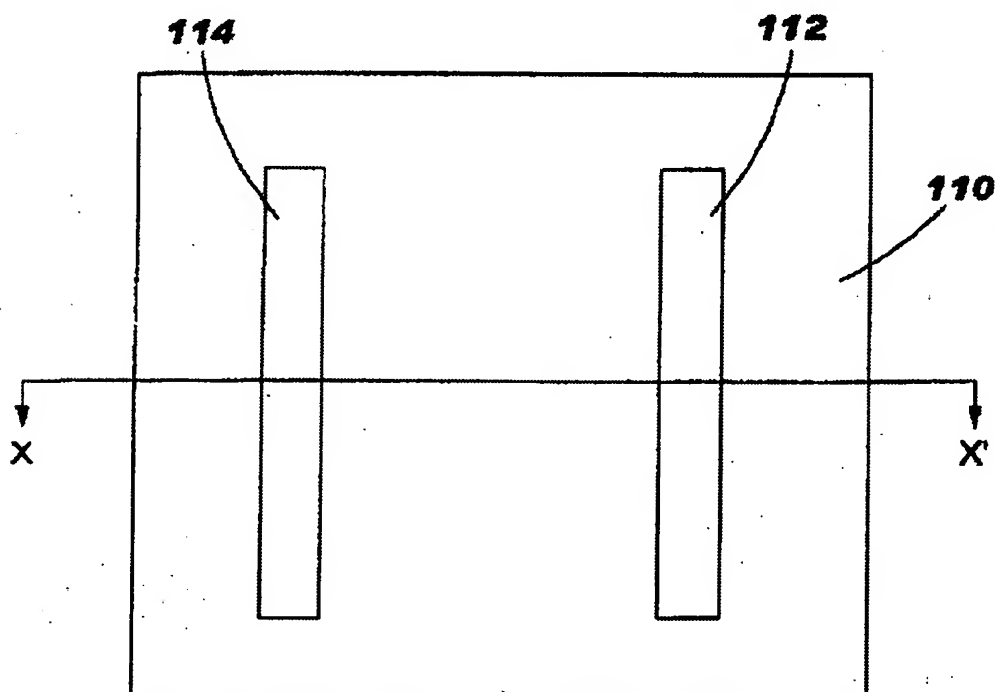


FIG. 2A

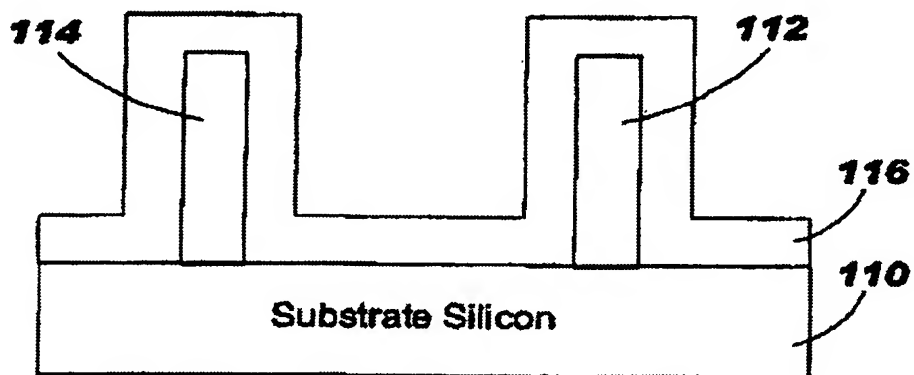
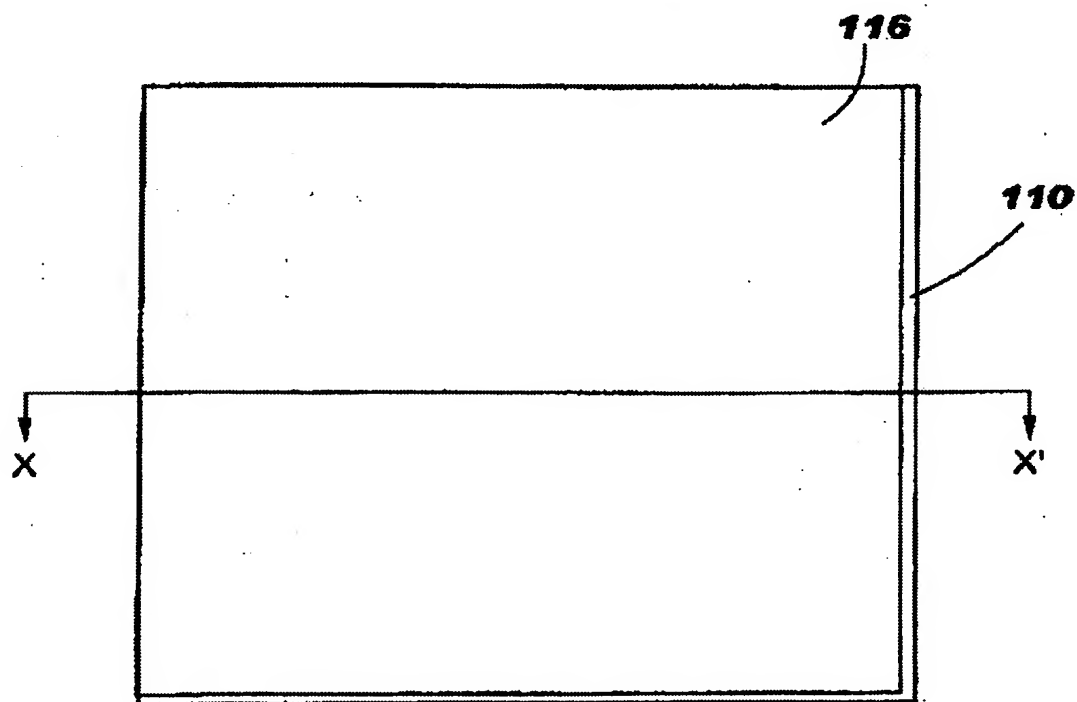


FIG. 2B



U.S. Patent

May 29, 2007

Sheet 3 of 15

7,224,029 B2

FIG. 3A

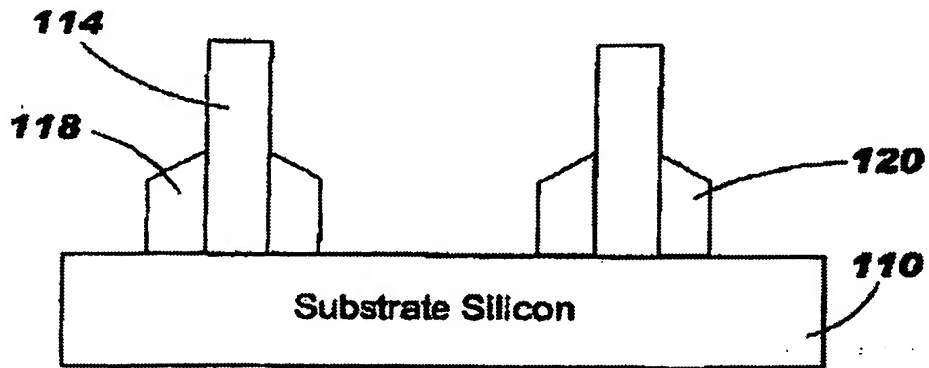


FIG. 3B

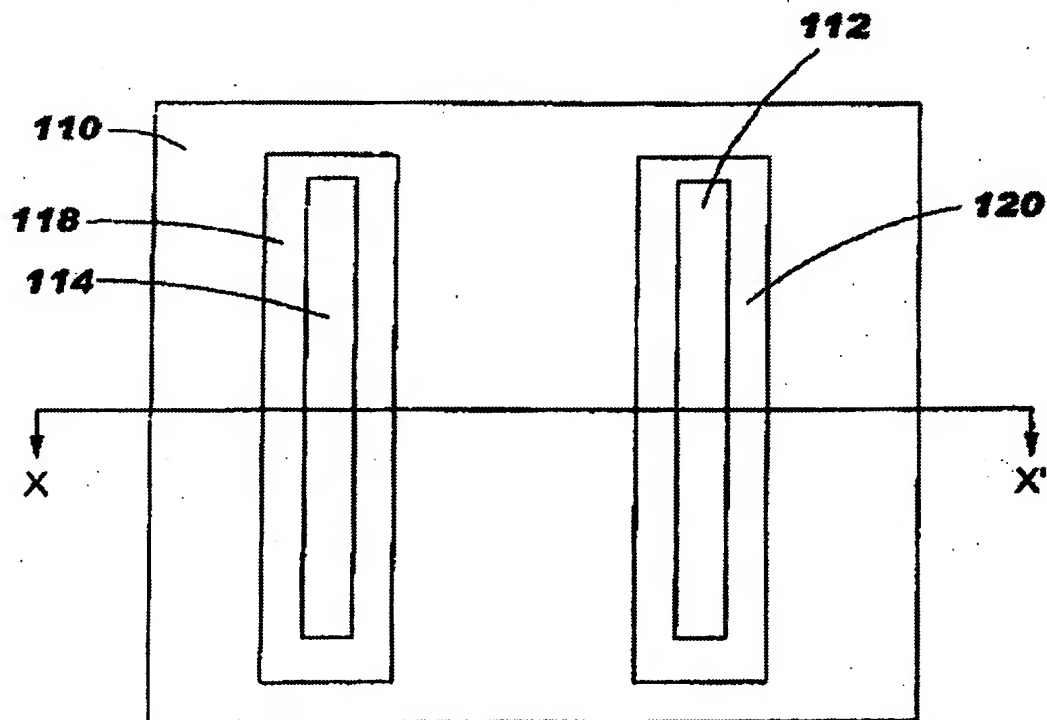


FIG. 4A

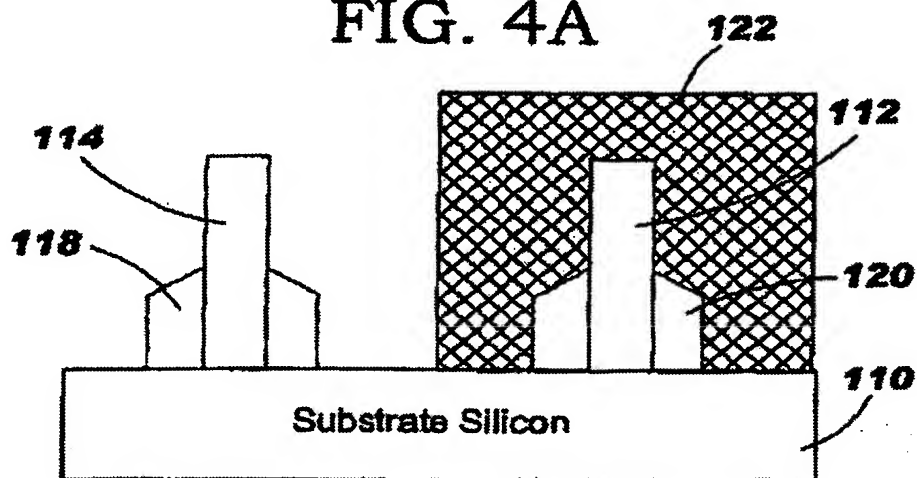


FIG. 4B

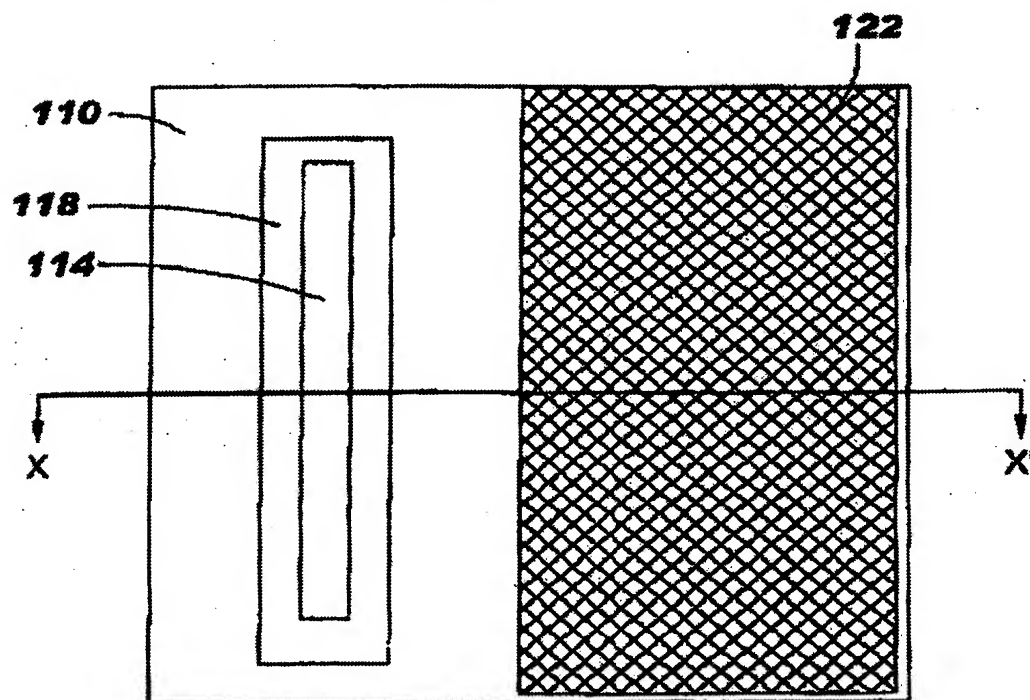


FIG. 5A

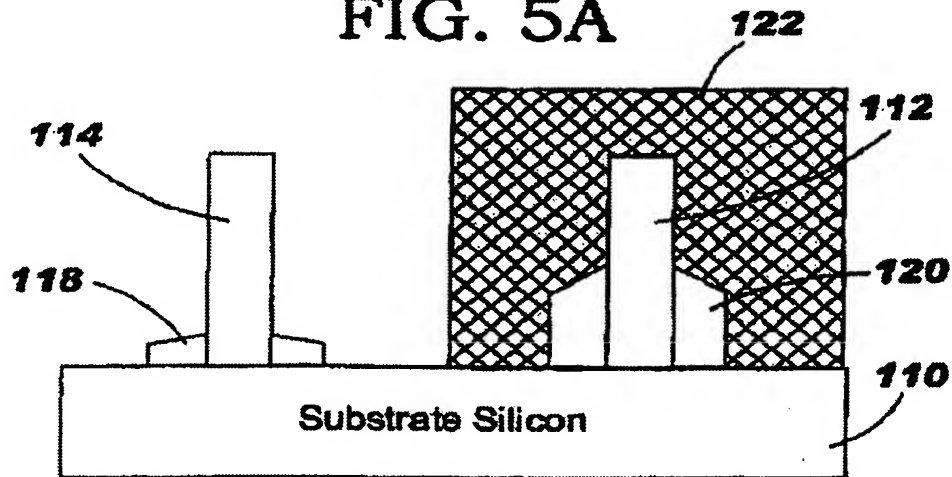


FIG. 5B

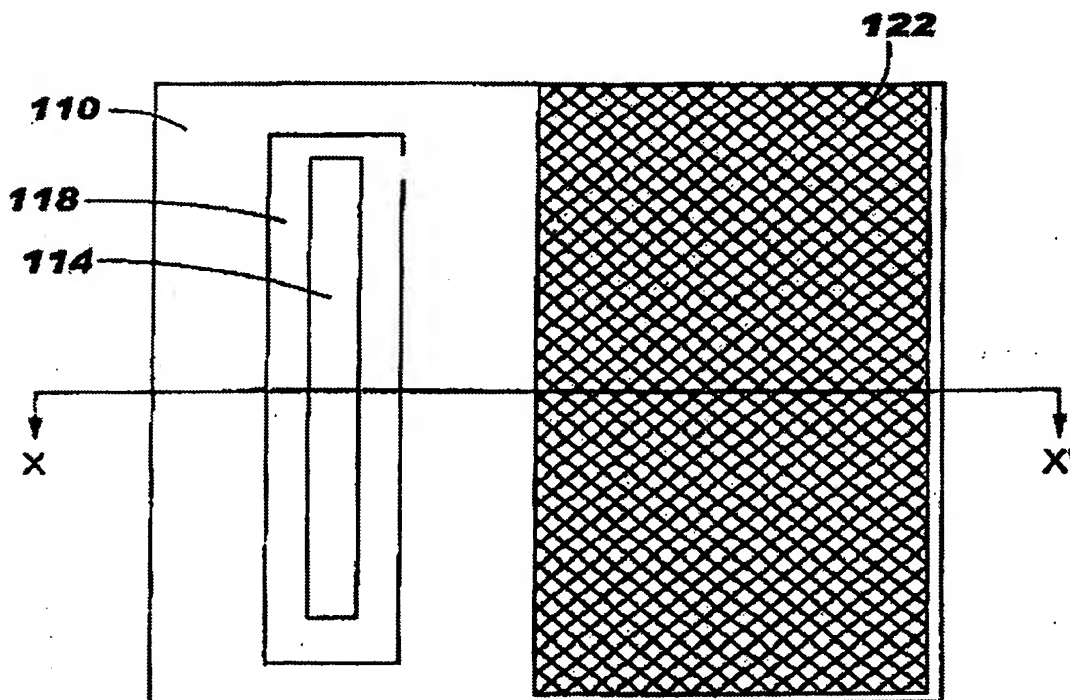


FIG. 6A

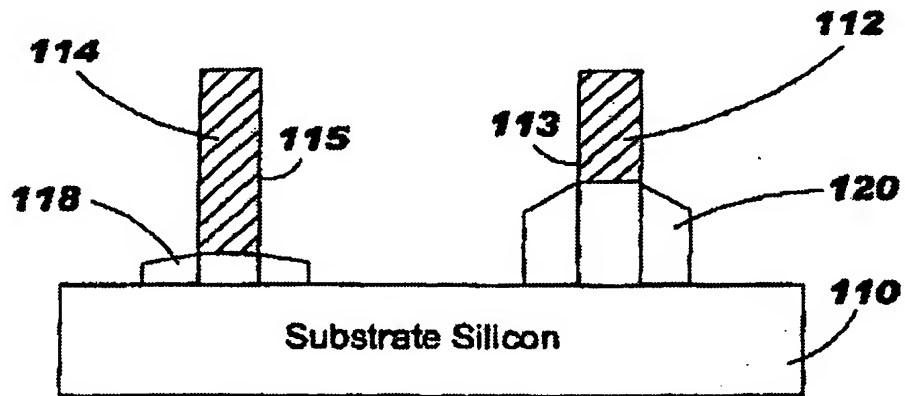


FIG. 6B

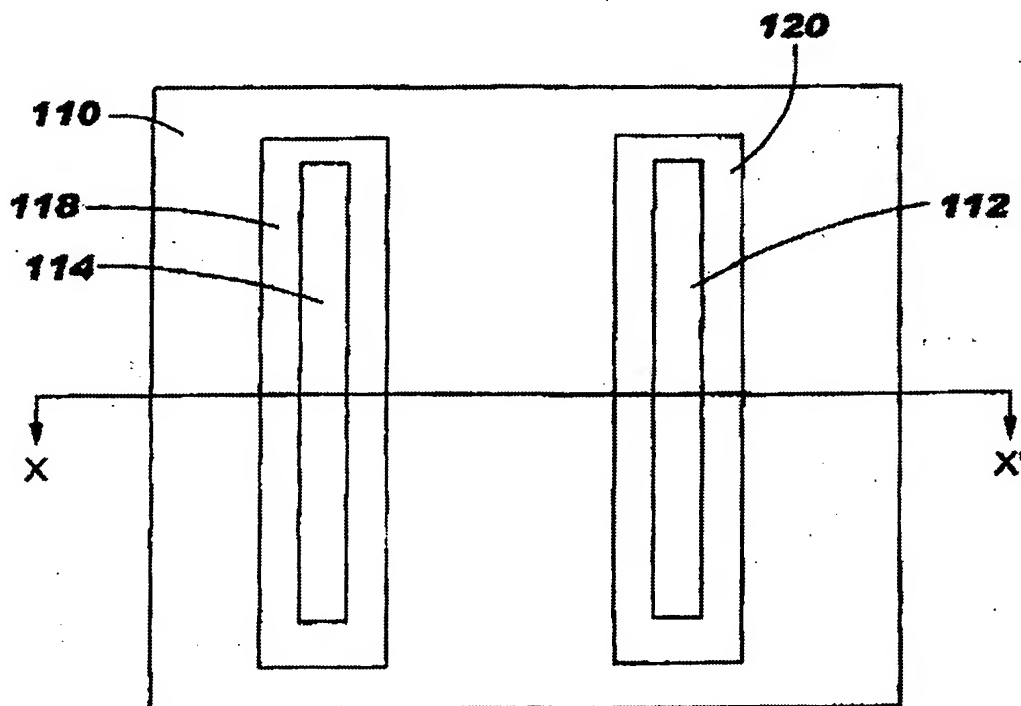




FIG. 7A

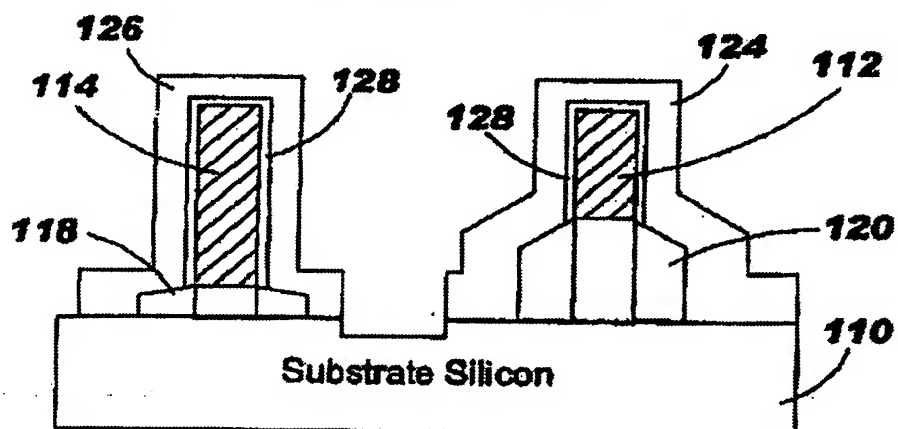


FIG. 7B

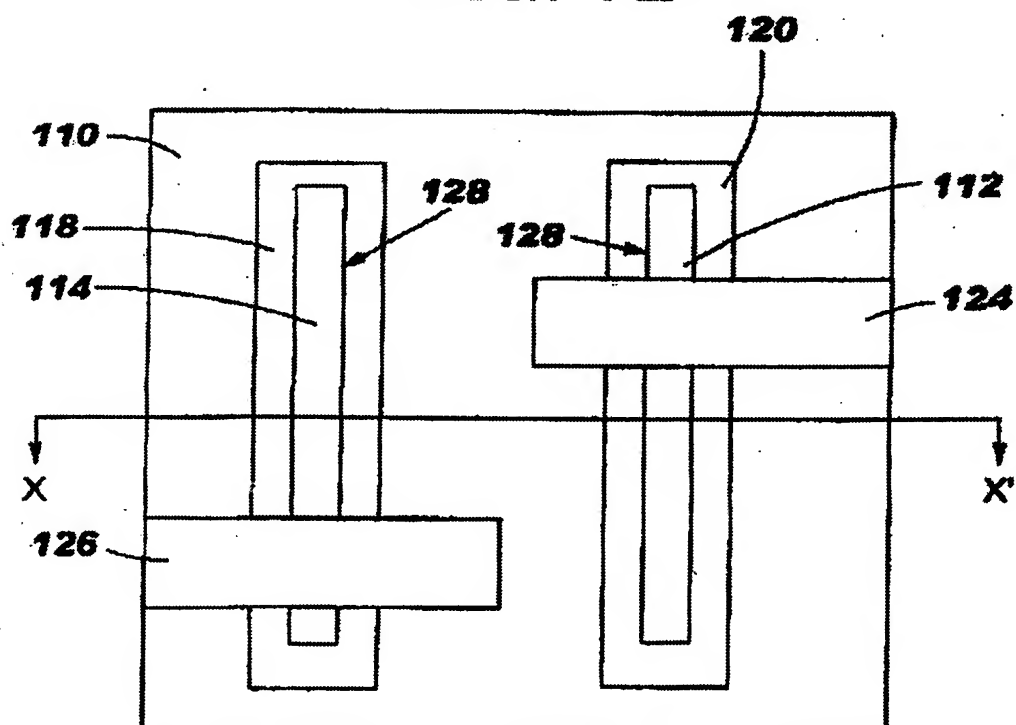


FIG. 8A

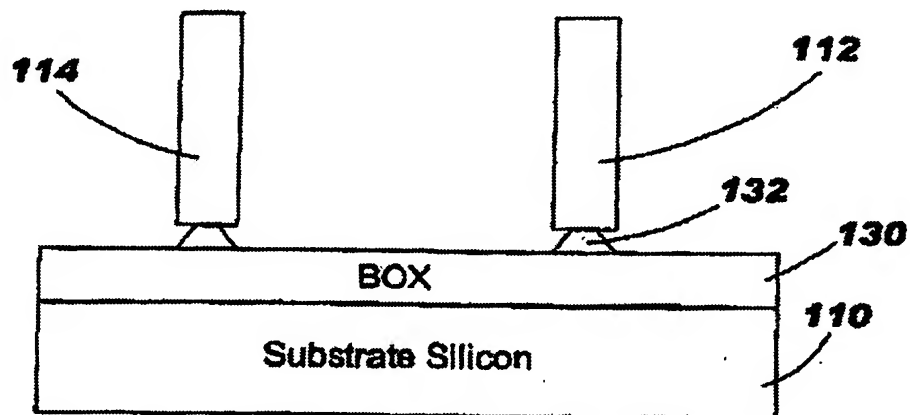
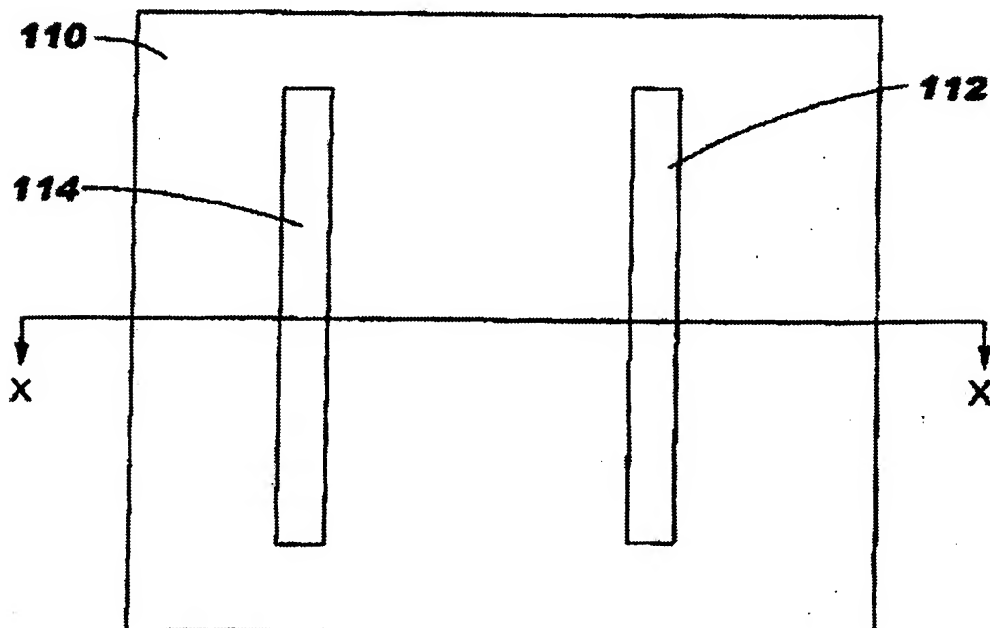


FIG. 8B



U.S. Patent

May 29, 2007

Sheet 9 of 15

7,224,029 B2

FIG. 9A

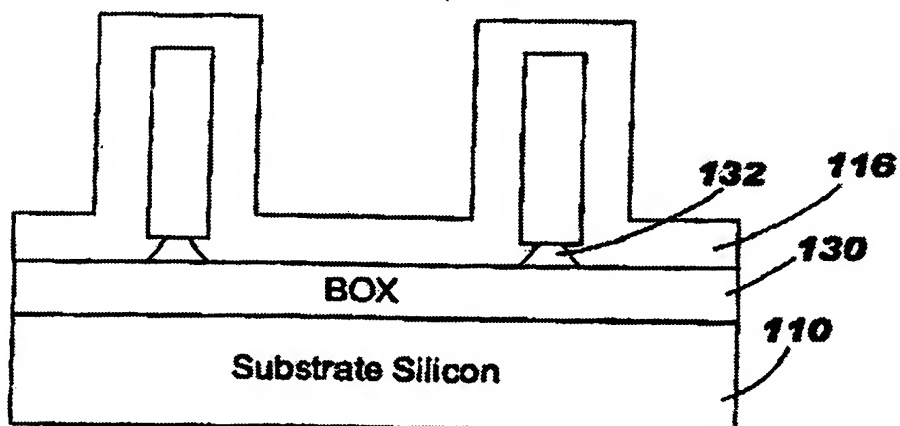


FIG. 9B

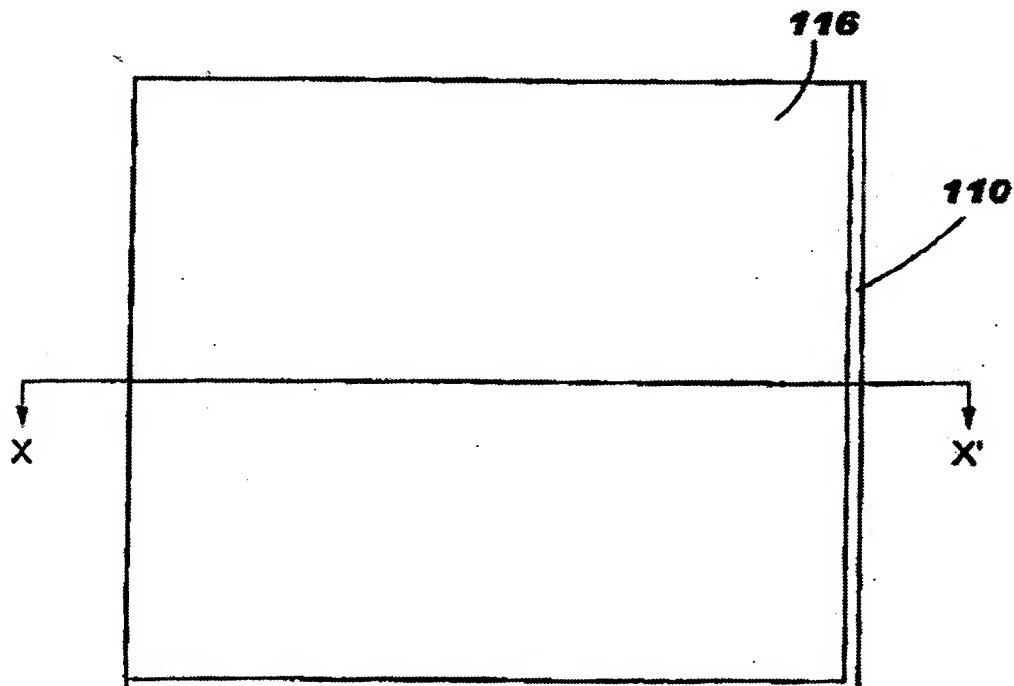


FIG. 10A

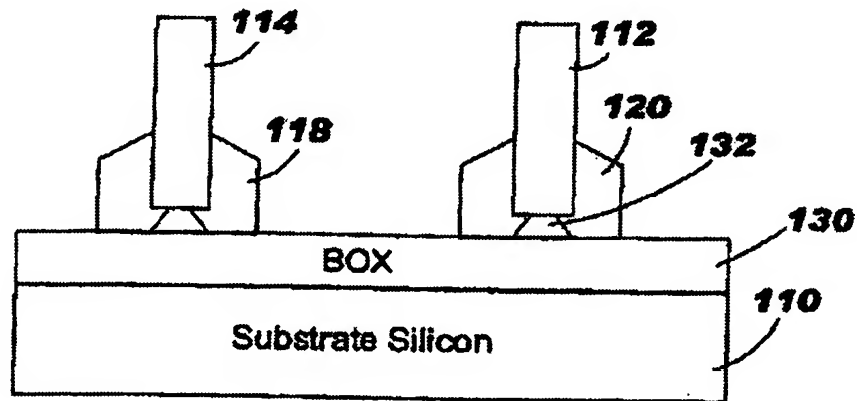


FIG. 10B

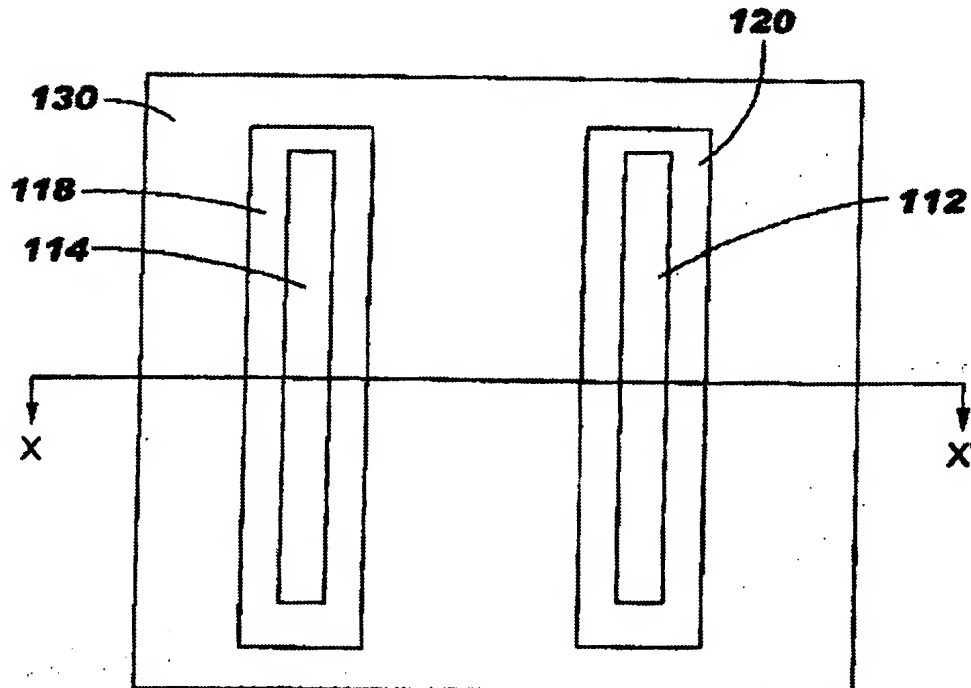


FIG. 11A

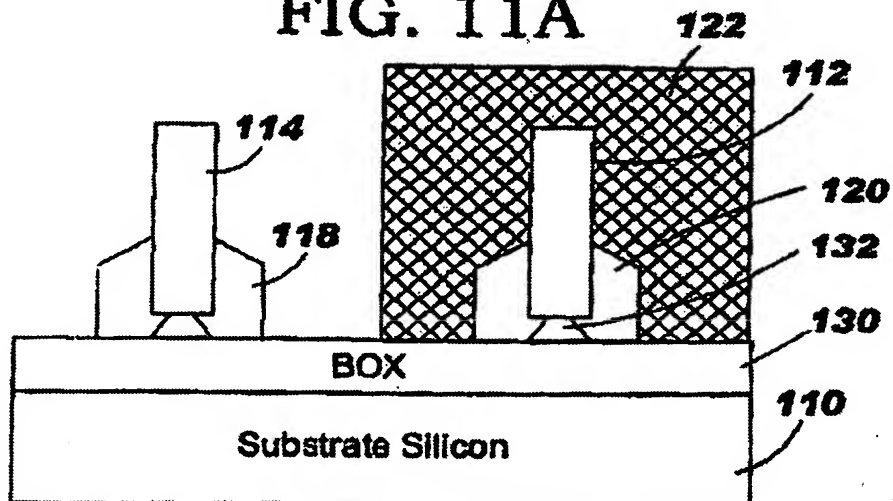
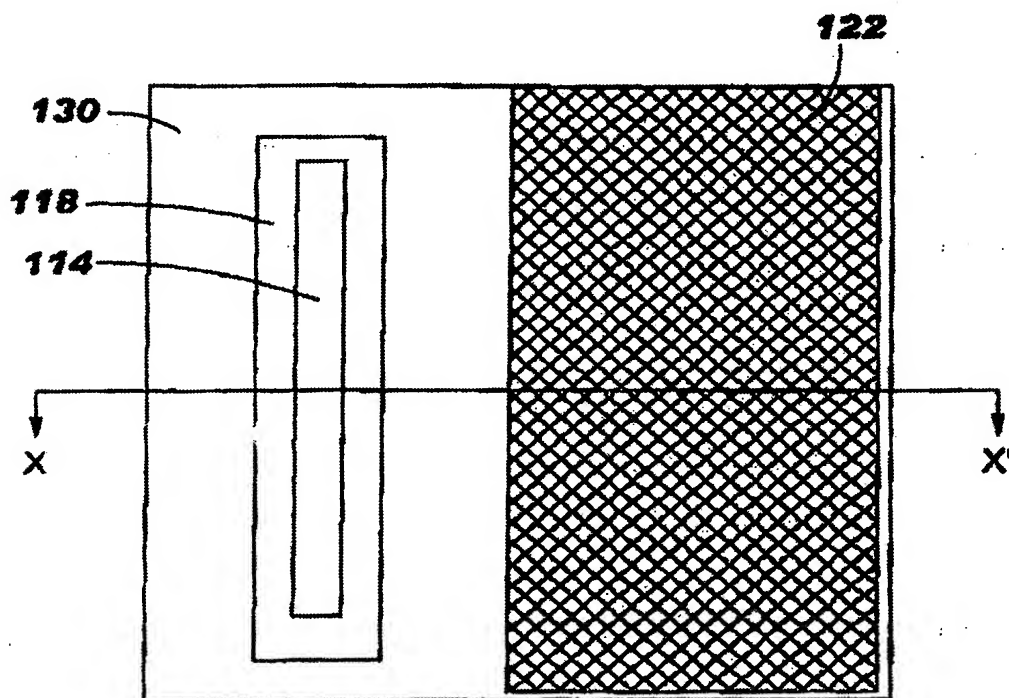


FIG. 11B



U.S. Patent

May 29, 2007

Sheet 12 of 15

7,224,029 B2

FIG. 12A

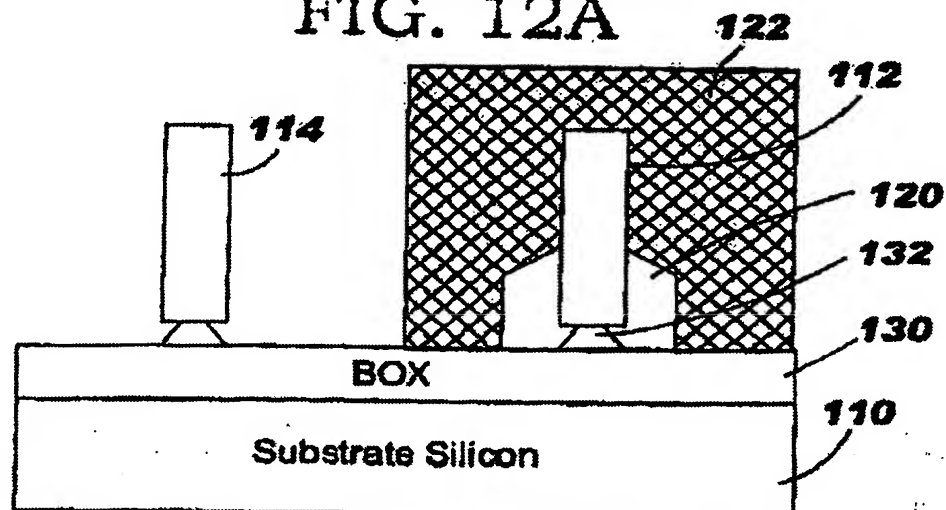


FIG. 12B

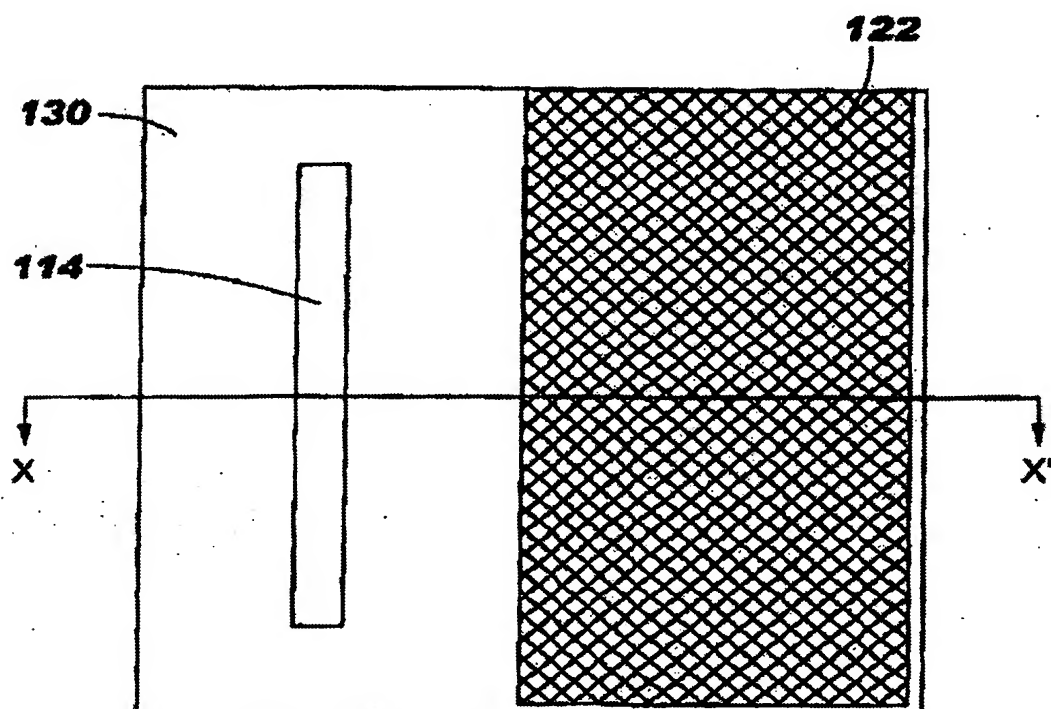


FIG. 13A

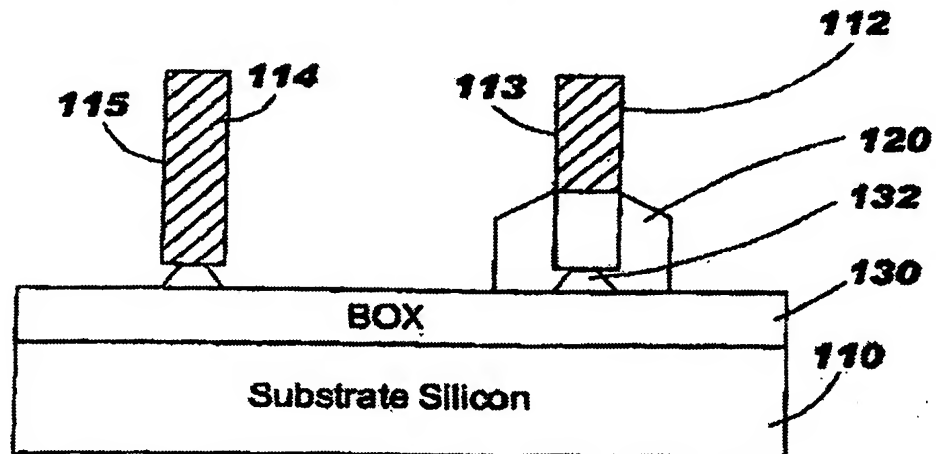


FIG. 13B

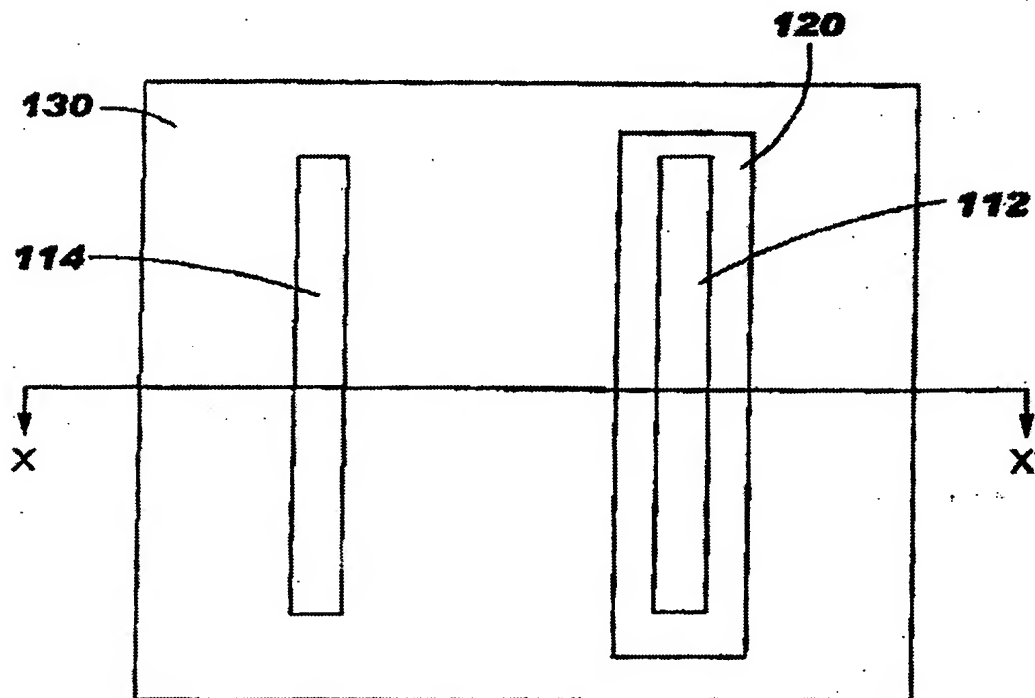


FIG. 14A

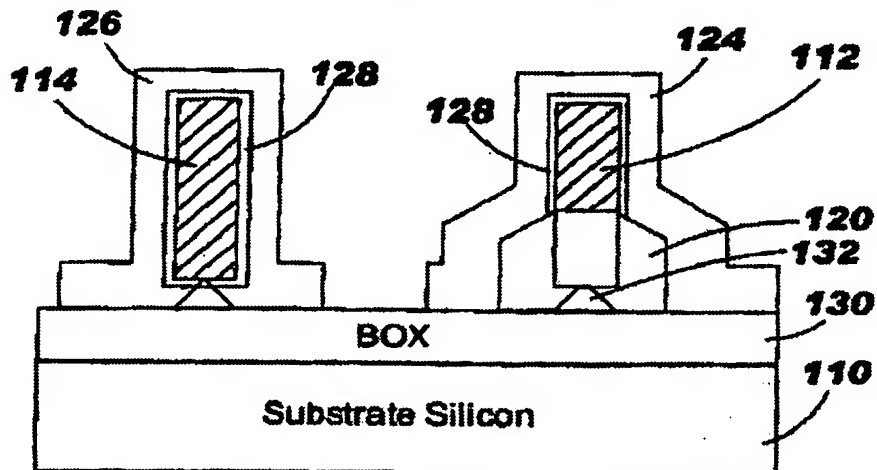


FIG. 14B

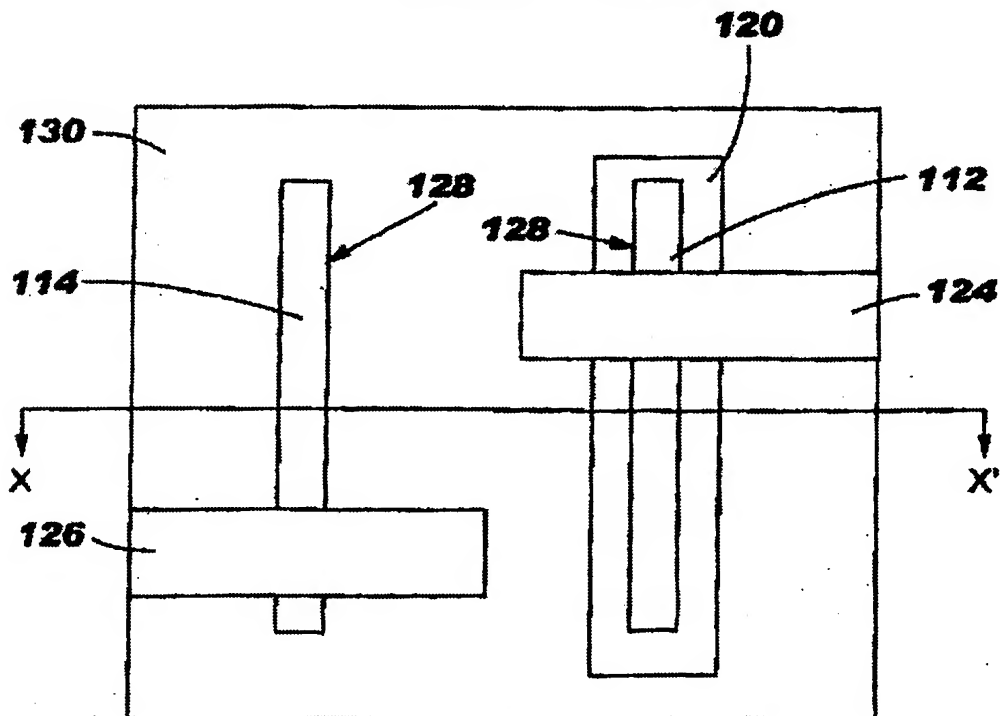




FIG. 15

